AMENDMENTS TO THE CLAIMS

1. (Original) A pulse wave Doppler application specific integrated circuit (PW-ASIC).

2. (Original) A combined pulse wave and continuous wave Doppler beam former application specific integrated circuit (PC-ASIC).

3. (Original) An ultrasound system application specific integrated circuit (US-ASIC) having at least one beam former, a transducer controller, one or more digital signal processor(s), and a plurality of input/output channels for linking to at least one memory means, a power control system, a transducer and a user interface.

4. (Previously Presented) The PW-ASIC of claim 1 comprises:

a transmit circuit; and

a delay circuit, wherein said delay circuit causes said transmit circuit to fire at a particular frequency.

5. (Previously Presented) The PW-ASIC of claim 4 further comprises:

a beam former.

6. (Previously Presented) The PW-ASIC of claim 5, wherein said beam former is used in providing pulse wave Doppler, B mode, and M mode image processing.

7. (Previously Presented) The PC-ASIC of claim 2 comprises:

a beam former.

8. (Previously Presented) The PC-ASIC of claim 7, wherein said beam former comprises:

a local oscillator generator.

9. (Previously Presented) The PC-ASIC of claim 7, wherein said beam former produces a complex base band output from an analog receive signal.

10. (Previously Presented) The PC-ASIC of claim 9, wherein said beam former comprises:

a sum circuit for the summation of base band signals of said complex base band output.

11. (Previously Presented) The PC-ASIC of claim 10, wherein said sum circuit comprises:

a filter to produce a base band beam formed signal.

12. (Previously Presented) The PC-ASIC of claim 2, wherein said PC-ASIC is part of a diagnostic medical ultrasound system.

13. (Previously Presented) The US-ASIC of claim 3, wherein said at least one beam former comprises:

a transmit beam former and a receive beam former.

14. (Previously Presented) The US-ASIC of claim 13, wherein said transmit beam former and said receive beam former draw from a single master clock path for precise timing.

15. (Previously Presented) The US-ASIC of claim 3, further comprising:

analog to digital and digital to analog converters.